April 12, 2003: AVIS'03 Final Programme

8:45 Welcome (R. Bharadwaj)

Session I: Software Model Checking

9:00 Software Model Checking of Safety and Liveness Properties
Andreas Podelski and Andrey Rybalchenko
(Max-Planck-Institut-für-Informatik, D) *(Invited)*

9:45 Control-flow in Software Model Checking – An Automata-Theoretic Approach
Javier Esparza (Universität Stuttgart, D) *(Invited)*

10:30 – 11:00 Coffee

Session II: Symbolic Methods

11:00 Verification of Embedded Systems with BDD-like Data Structures
Farn Wang (National Taiwan University, TWN) *(Invited)*

11:45 A Symbolic Representation of Unbounded Queue Contents by a Finite Union of DFAs
Suman Roy (Satyam Computer Services Ltd., IN)

12:15 Fatalis: Real-Time Processes as Linear Logic Specifications
Jean-Pierre Jouannaud (LIX, École Polytechnique, F) *(Invited)*

13:00 – 14:30 Lunch

Session III: Practical Applications

14:30 From Requirements Specification to Code Verification: A Functional Approach
Jan Madey (Warsaw University, PL) *(Invited)*

15:15 Property Preserving Abstraction for Software Verification – A Case Study
Thomas Firley and Ursula Goltz (Technical University Braunschweig, D)

16:00 – 16:30 Coffee

Session IV: Security Protocols

16:30 An Equivalence on Terms for Security Protocols
R. Ramanujam and **S.P.Suresh** (Institute of Mathematical Sciences, IN)

Session V: Refinement

17:00 In-place Refinement for Effect Checking
Viktor Kuncak and K. Rustan M. Leino
(Massachusetts Institute of Technology and Microsoft Research, USA)

17:30 Formal Refinement Verification Method of Real-Time Systems with Discrete Probability Distributions
Satoshi Yamane (Kanazawa University, JP)